FIG. 1

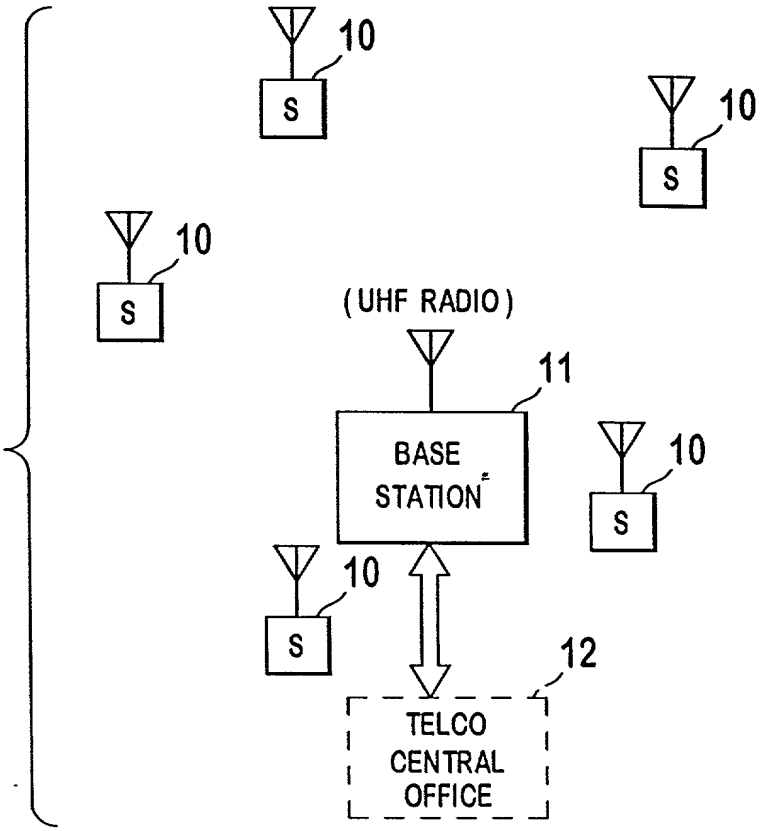
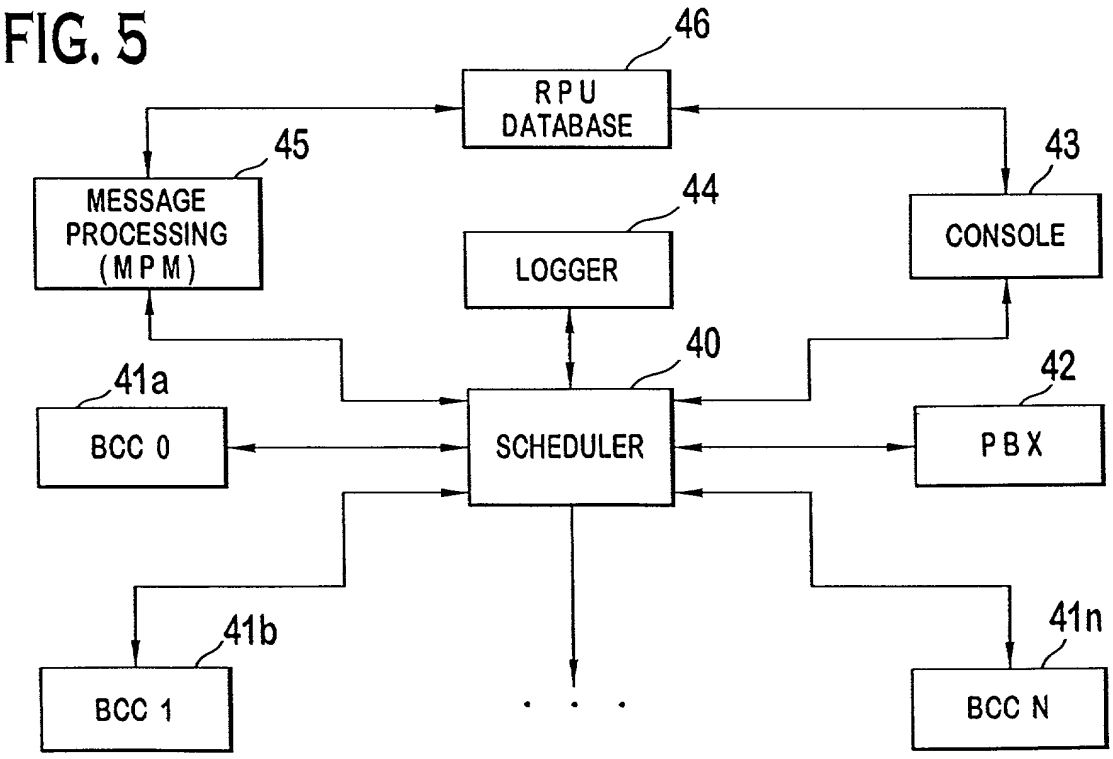

10
S
10
S
10
S
(UHF RADIO)
11
BASE STATION
10
S
10
S
12
TELCO CENTRAL OFFICE

FIG. 5


46
RPU DATABASE
45
MESSAGE PROCESSING (MPM)
44
LOGGER
43
CONSOLE
40
41a
BCC 0
SCHEDULER
42
PBX
41b
BCC 1
41n
BCC N

EP 0 980 187 A2

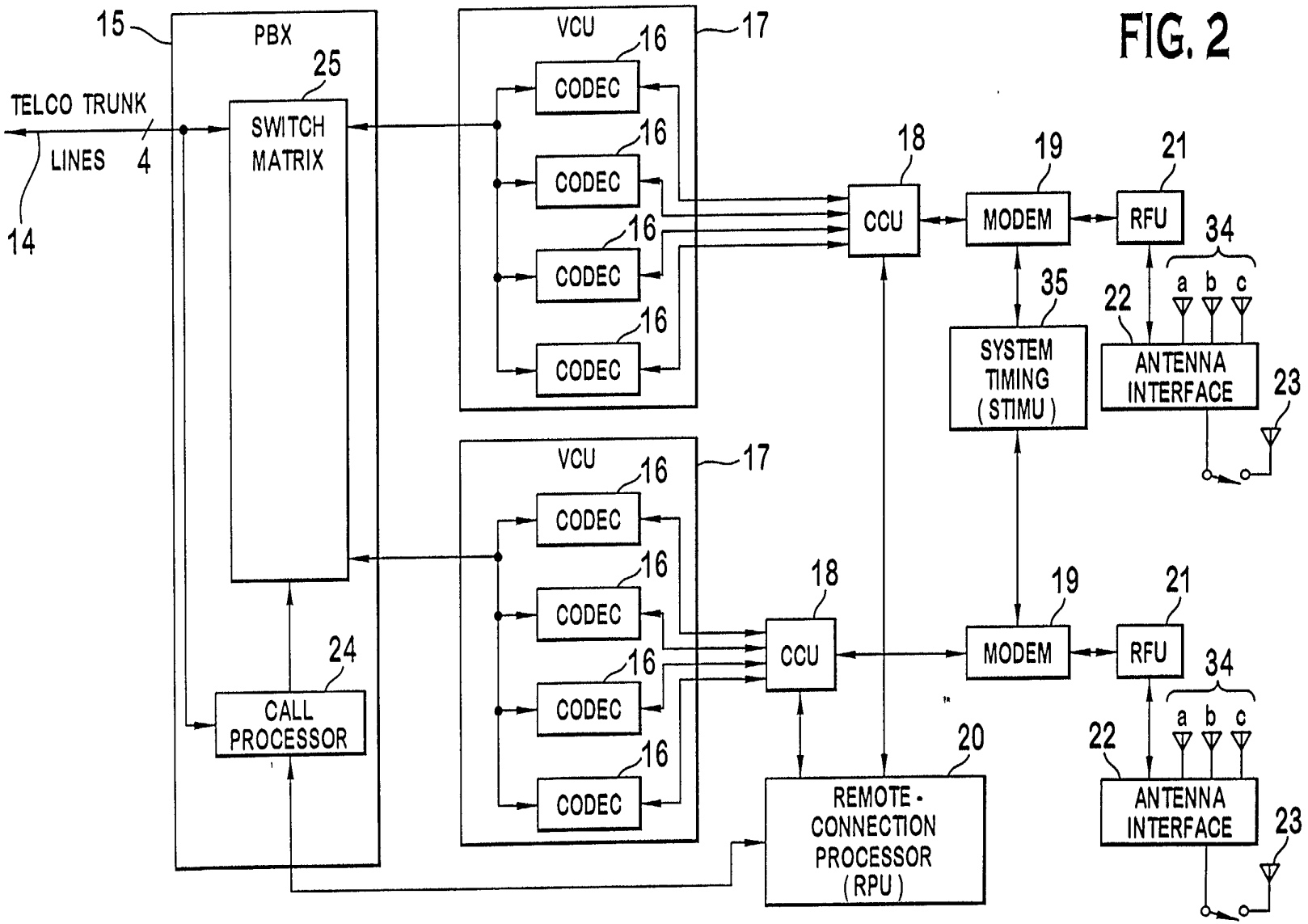


FIG. 2

FIG. 3

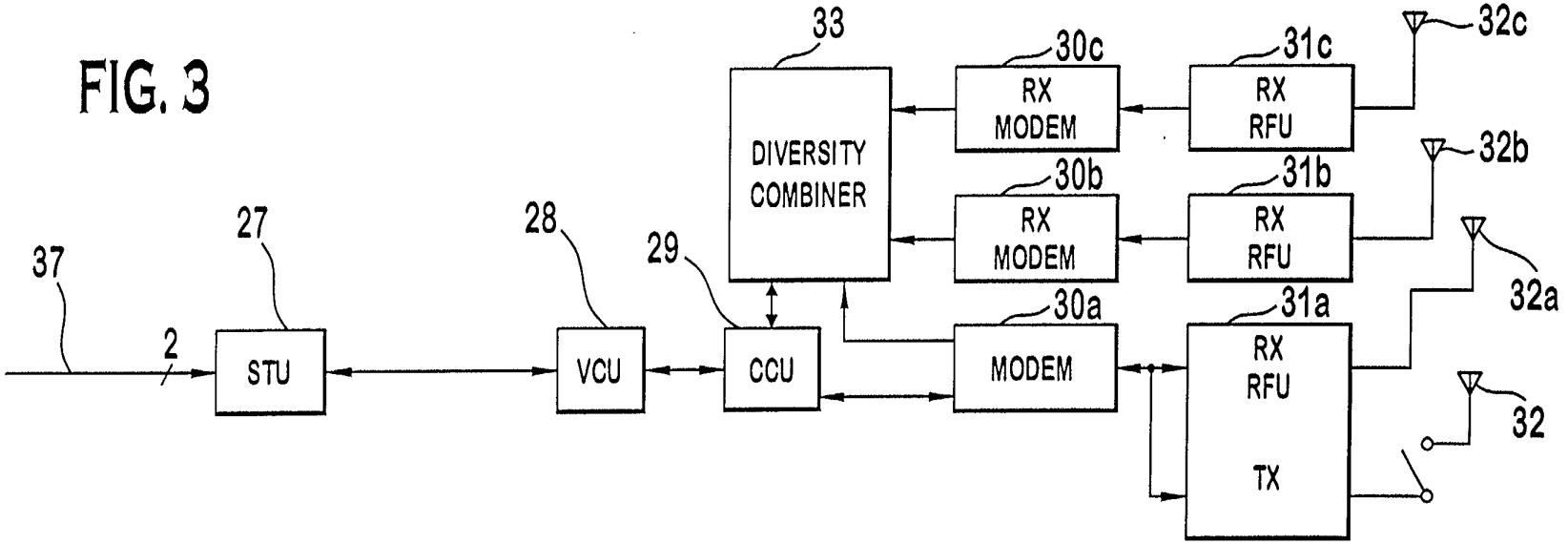

33
30c
31c
32c
DIVERSITY COMBINER
RX MODEM
RX RFU
30b
31b
32b
RX MODEM
RX RFU
27
28
29
37
2
32a
30a
31a
STU
VCU
CCU
MODEM
RX RFU
32
TX

FIG. 25

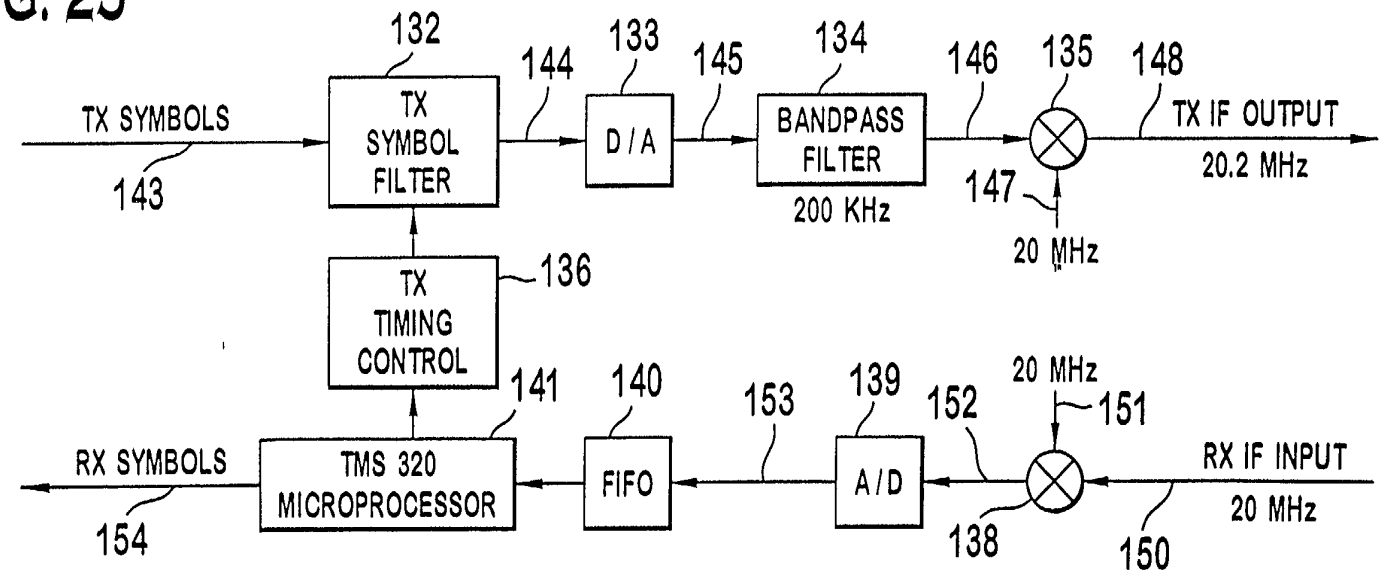
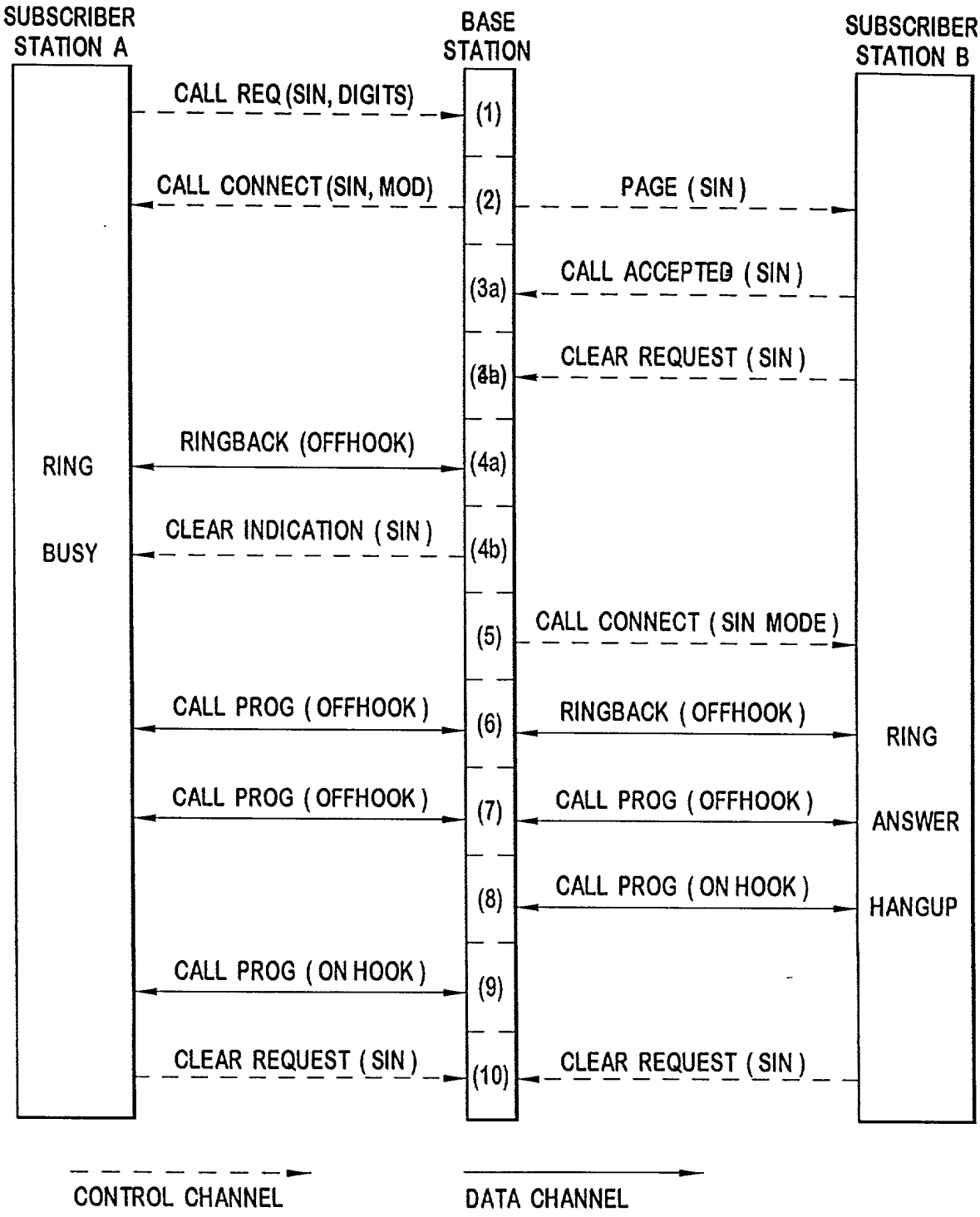

132
144
133
145
134
146
135
148
TX SYMBOLS
TX SYMBOL FILTER
D/A
BANDPASS FILTER
TX IF OUTPUT
143
200 KHz
147
20.2 MHz
20 MHz
TX TIMING CONTROL
136
141
140
153
139
152
20 MHz
151
RX SYMBOLS
TMS 320 MICROPROCESSOR
FIFO
A/D
RX IF INPUT
154
138
150
20 MHz

FIG. 4


SUBSCRIBER STATION A
BASE STATION
SUBSCRIBER STATION B
CALL REQ (SIN, DIGITS)
(1)
CALL CONNECT (SIN, MOD)
(2)
PAGE (SIN)
CALL ACCEPTED (SIN)
(3a)
CLEAR REQUEST (SIN)
(3a)
RINGBACK (OFFHOOK)
RING
(4a)
CLEAR INDICATION (SIN)
BUSY
(4b)
CALL CONNECT (SIN MODE)
(5)
CALL PROG (OFFHOOK)
(6)
RINGBACK (OFFHOOK)
RING
CALL PROG (OFFHOOK)
(7)
CALL PROG (OFFHOOK)
ANSWER
CALL PROG (ON HOOK)
(8)
HANGUP
CALL PROG (ON HOOK)
(9)
CLEAR REQUEST (SIN)
(10)
CLEAR REQUEST (SIN)
CONTROL CHANNEL
DATA CHANNEL

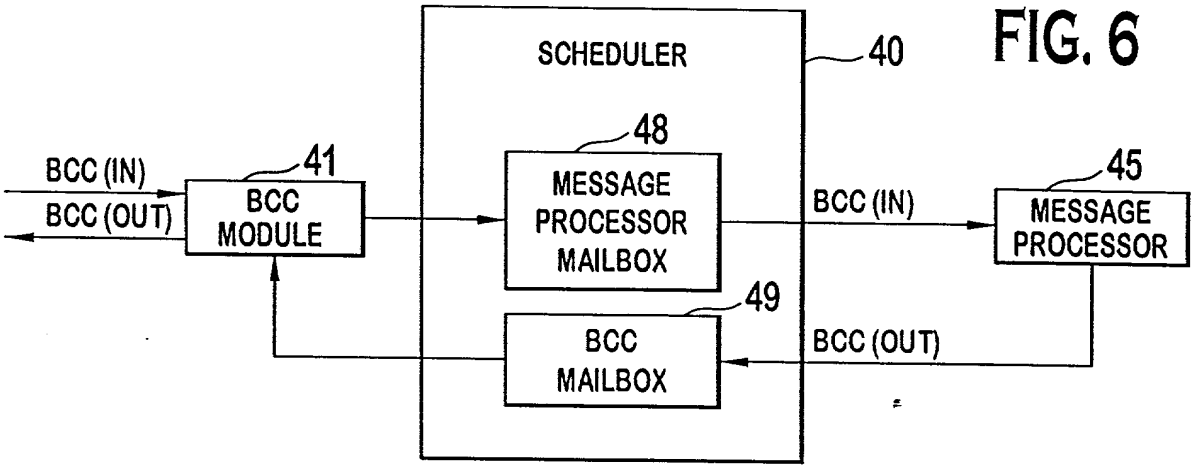


FIG. 6

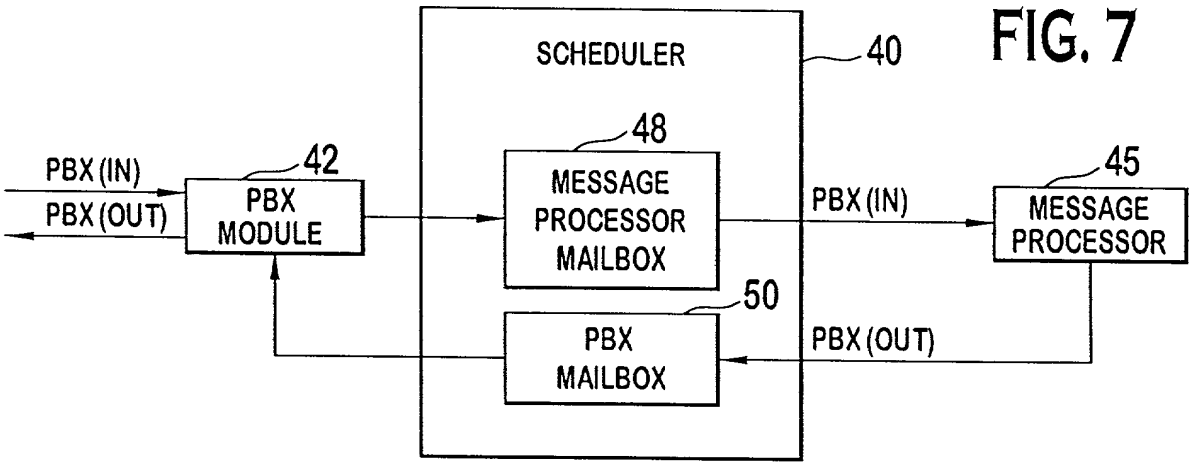


FIG. 7

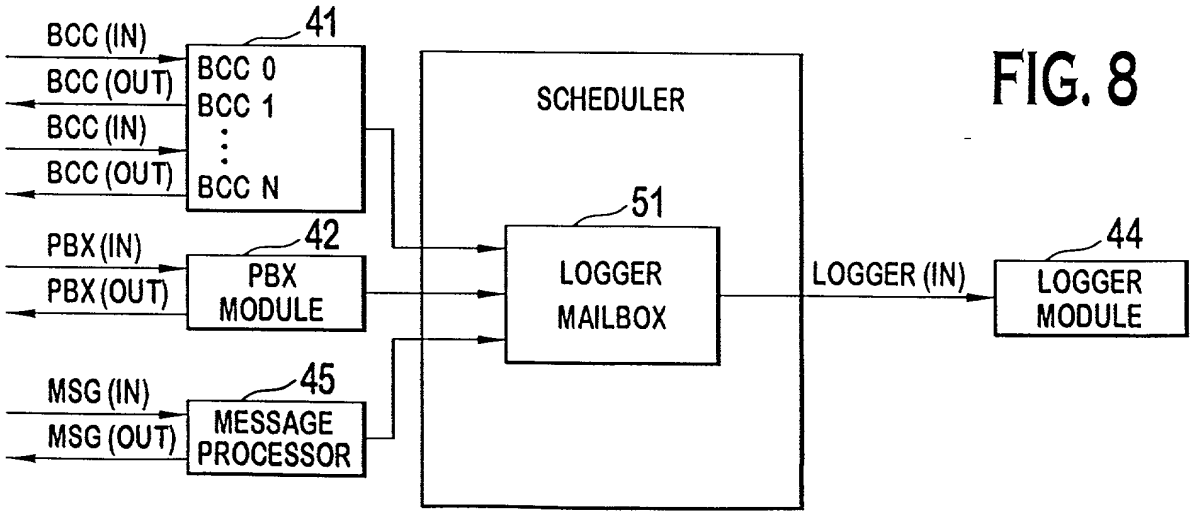


FIG. 8

FIG. 9

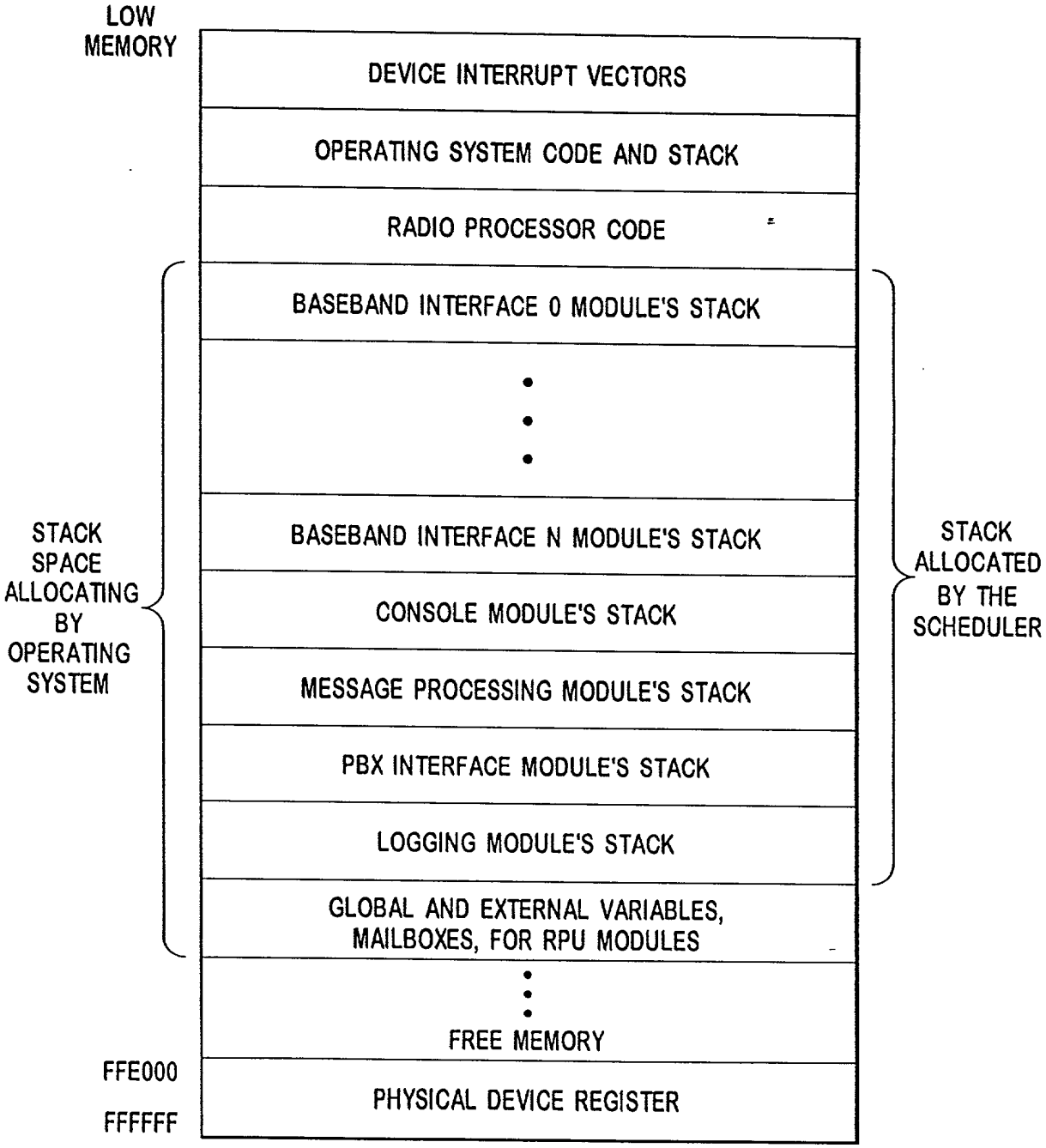
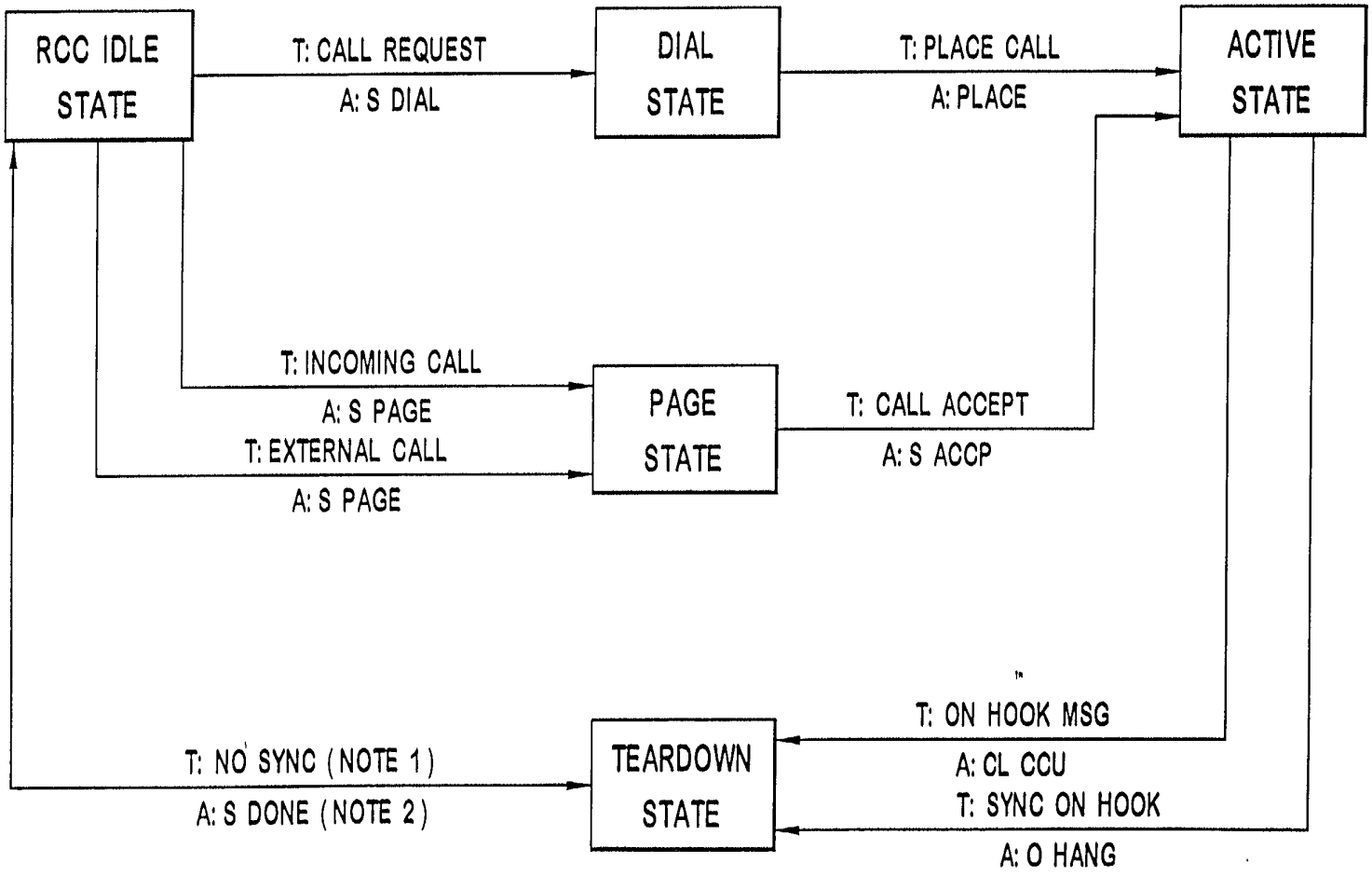

LOW MEMORY
DEVICE INTERRUPT VECTORS
OPERATING SYSTEM CODE AND STACK
RADIO PROCESSOR CODE
BASEBAND INTERFACE 0 MODULE'S STACK
BASEBAND INTERFACE N MODULE'S STACK
CONSOLE MODULE'S STACK
MESSAGE PROCESSING MODULE'S STACK
PBX INTERFACE MODULE'S STACK
LOGGING MODULE'S STACK
GLOBAL AND EXTERNAL VARIABLES, MAILBOXES, FOR RPU MODULES
FREE MEMORY
PHYSICAL DEVICE REGISTER
FFE000
FFFFFF
STACK SPACE ALLOCATING BY OPERATING SYSTEM
STACK ALLOCATED BY THE SCHEDULER

FIG. 10


RCC IDLE STATE
T: CALL REQUEST
A: S DIAL
DIAL STATE
T: PLACE CALL
A: PLACE
ACTIVE STATE
T: INCOMING CALL
A: S PAGE
T: EXTERNAL CALL
A: S PAGE
PAGE STATE
T: CALL ACCEPT
A: S ACCP
T: ON HOOK MSG
A: CL CCU
T: SYNC ON HOOK
A: O HANG
T: NO SYNC (NOTE 1)
A: S DONE (NOTE 2)
TEARDOWN STATE

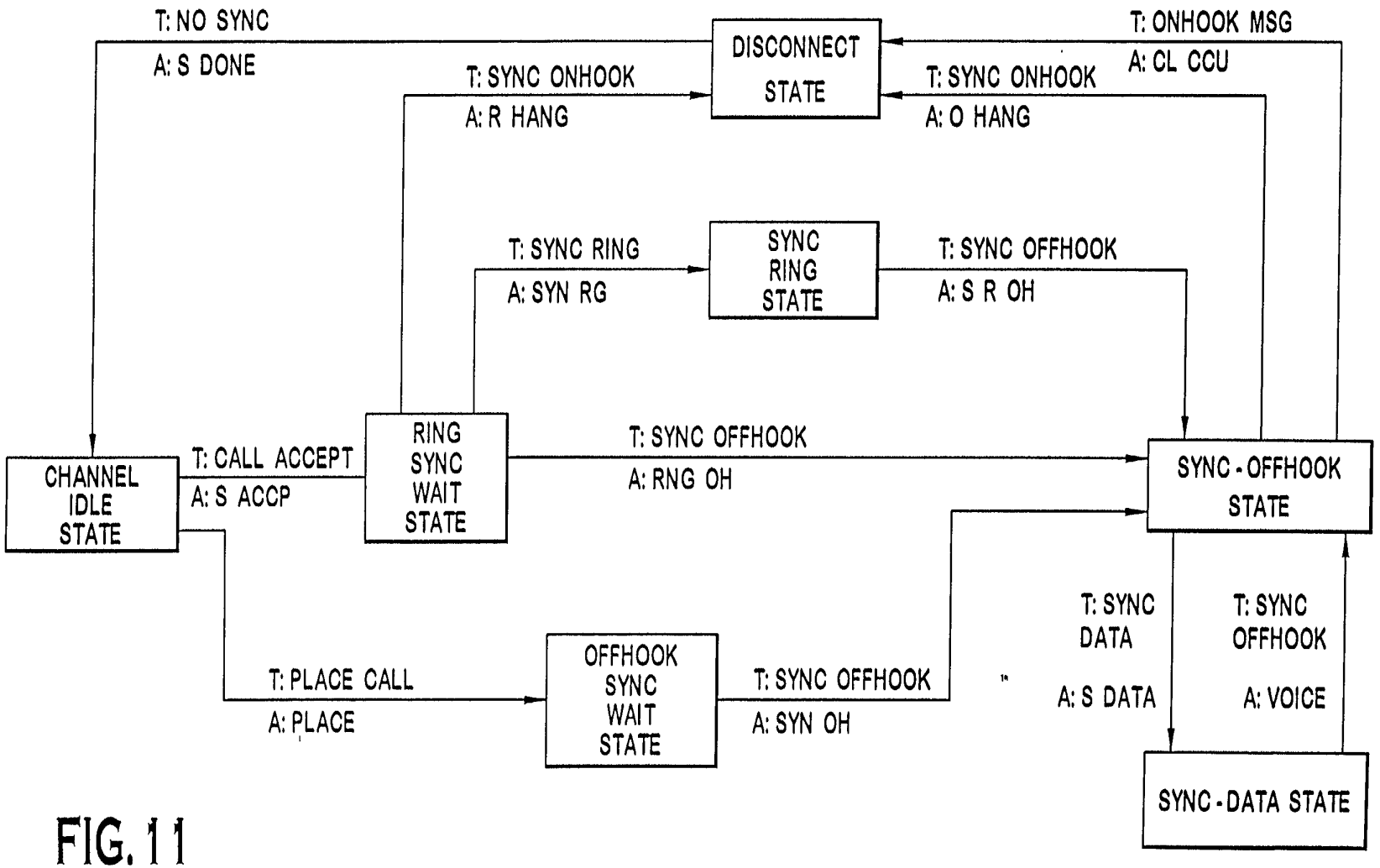
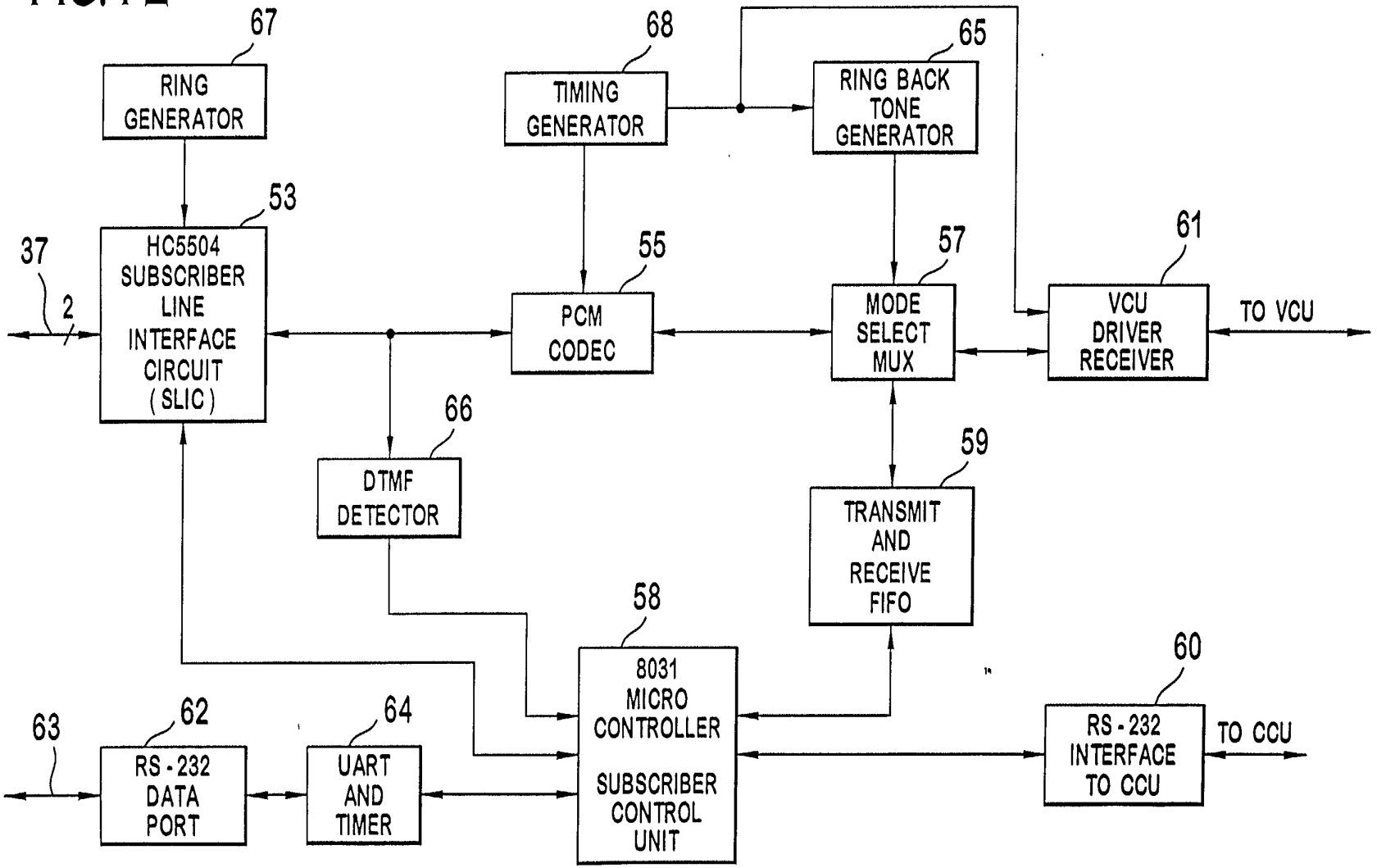

T: NO SYNC
A: S DONE
DISCONNECT STATE
T: ONHOOK MSG
A: CL CCU
T: SYNC ONHOOK
A: R HANG
T: SYNC ONHOOK
A: O HANG
T: SYNC RING
A: SYN RG
SYNC RING STATE
T: SYNC OFFHOOK
A: S R OH
CHANNEL IDLE STATE
T: CALL ACCEPT
A: S ACCP
RING SYNC WAIT STATE
T: SYNC OFFHOOK
A: RNG OH
SYNC - OFFHOOK STATE
T: SYNC DATA
A: S DATA
T: SYNC OFFHOOK
A: VOICE
T: PLACE CALL
A: PLACE
OFFHOOK SYNC WAIT STATE
T: SYNC OFFHOOK
A: SYN OH
SYNC - DATA STATE

FIG. 11

FIG. 12


67
RING GENERATOR
68
TIMING GENERATOR
65
RING BACK TONE GENERATOR
53
37
2
HC5504 SUBSCRIBER LINE INTERFACE CIRCUIT (SLIC)
55
PCM CODEC
57
MODE SELECT MUX
61
VCU DRIVER RECEIVER
TO VCU
66
DTMF DETECTOR
59
TRANSMIT AND RECEIVE FIFO
58
8031 MICRO CONTROLLER
SUBSCRIBER CONTROL UNIT
60
RS-232 INTERFACE TO CCU
TO CCU
63
62
RS-232 DATA PORT
64
UART AND TIMER

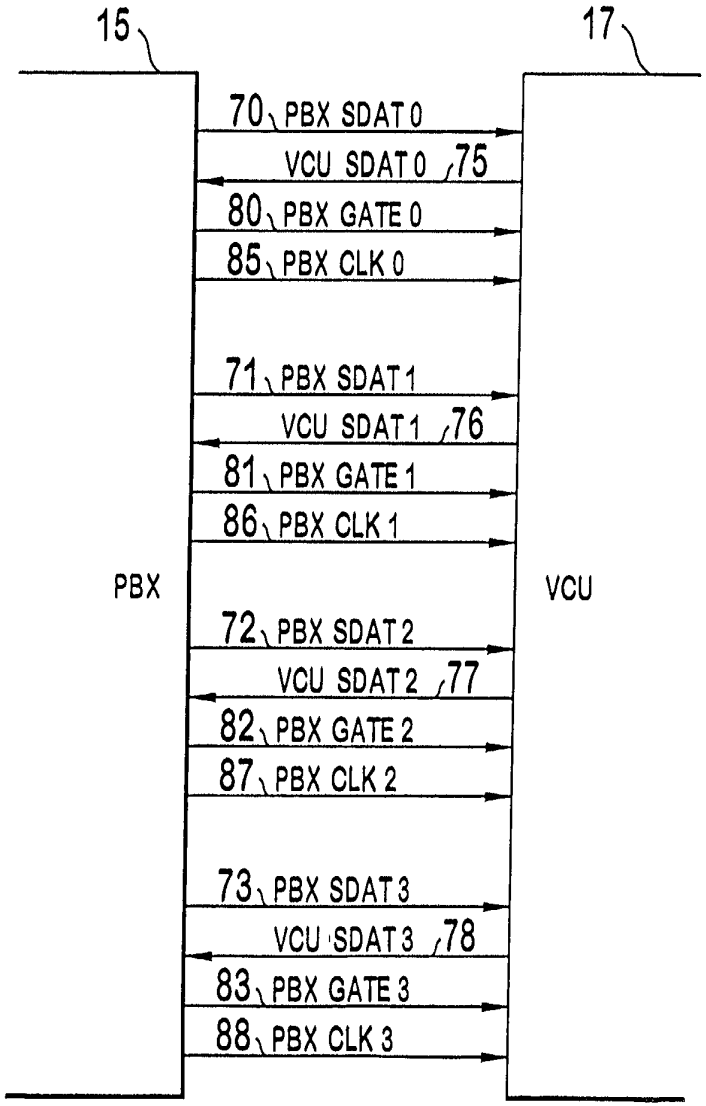

15
17
70 PBX SDAT 0
VCU SDAT 0 75
80 PBX GATE 0
85 PBX CLK 0
71 PBX SDAT 1
VCU SDAT 1 76
81 PBX GATE 1
86 PBX CLK 1
72 PBX SDAT 2
VCU SDAT 2 77
82 PBX GATE 2
87 PBX CLK 2
73 PBX SDAT 3
VCU SDAT 3 78
83 PBX GATE 3
88 PBX CLK 3
PBX
VCU

FIG. 13

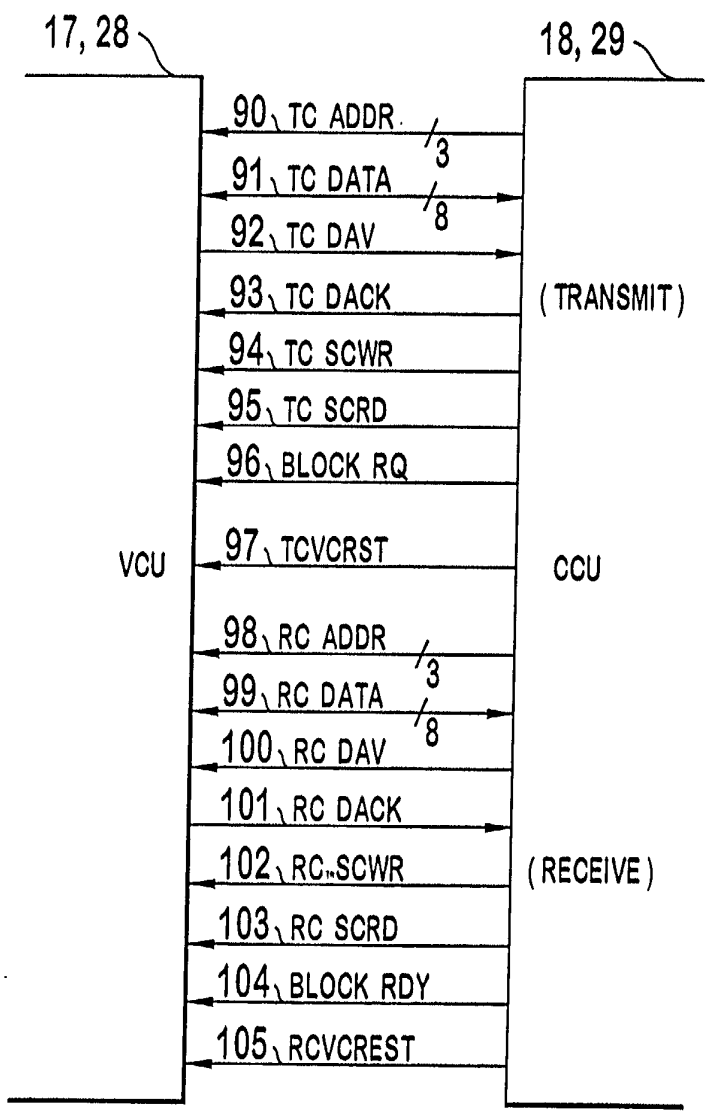

17, 28
18, 29
90 TC ADDR /3
91 TC DATA /8
92 TC DAV
93 TC DACK
94 TC SCWR
95 TC SCRD
96 BLOCK RQ
97 TCVCRST
98 RC ADDR /3
99 RC DATA /8
100 RC DAV
101 RC DACK
102 RC SCWR
103 RC SCRD
104 BLOCK RDY
105 RCVCREST
(TRANSMIT)
(RECEIVE)
VCU
CCU

FIG. 16

FIG. 14

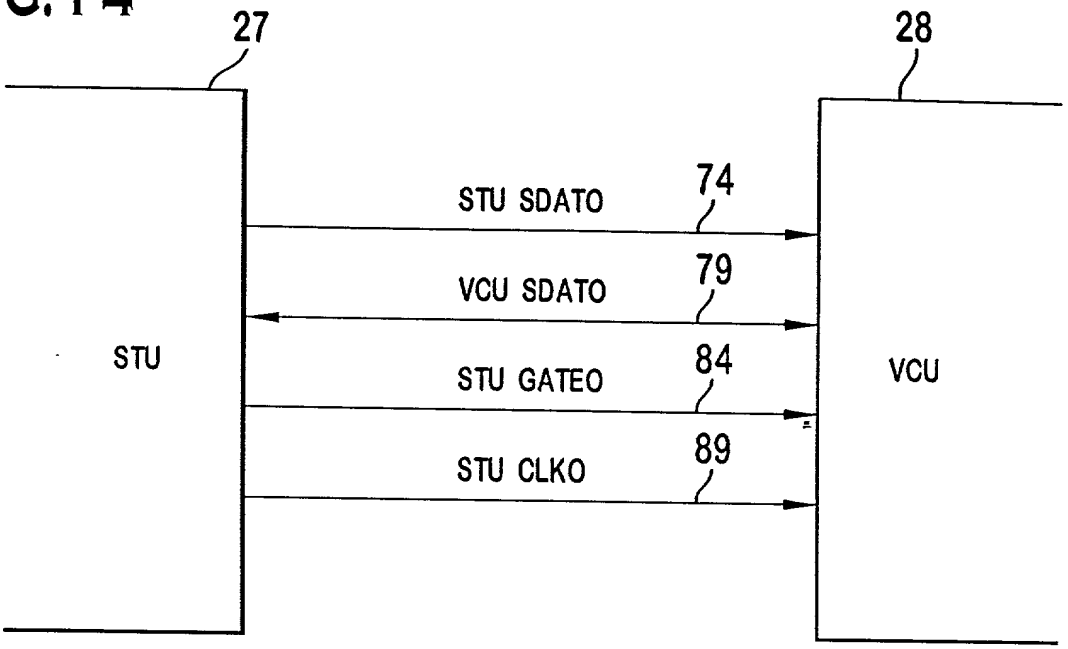

27
28
STU SDATO
74
VCU SDATO
79
STU
VCU
STU GATEO
84
STU CLKO
89

FIG. 21

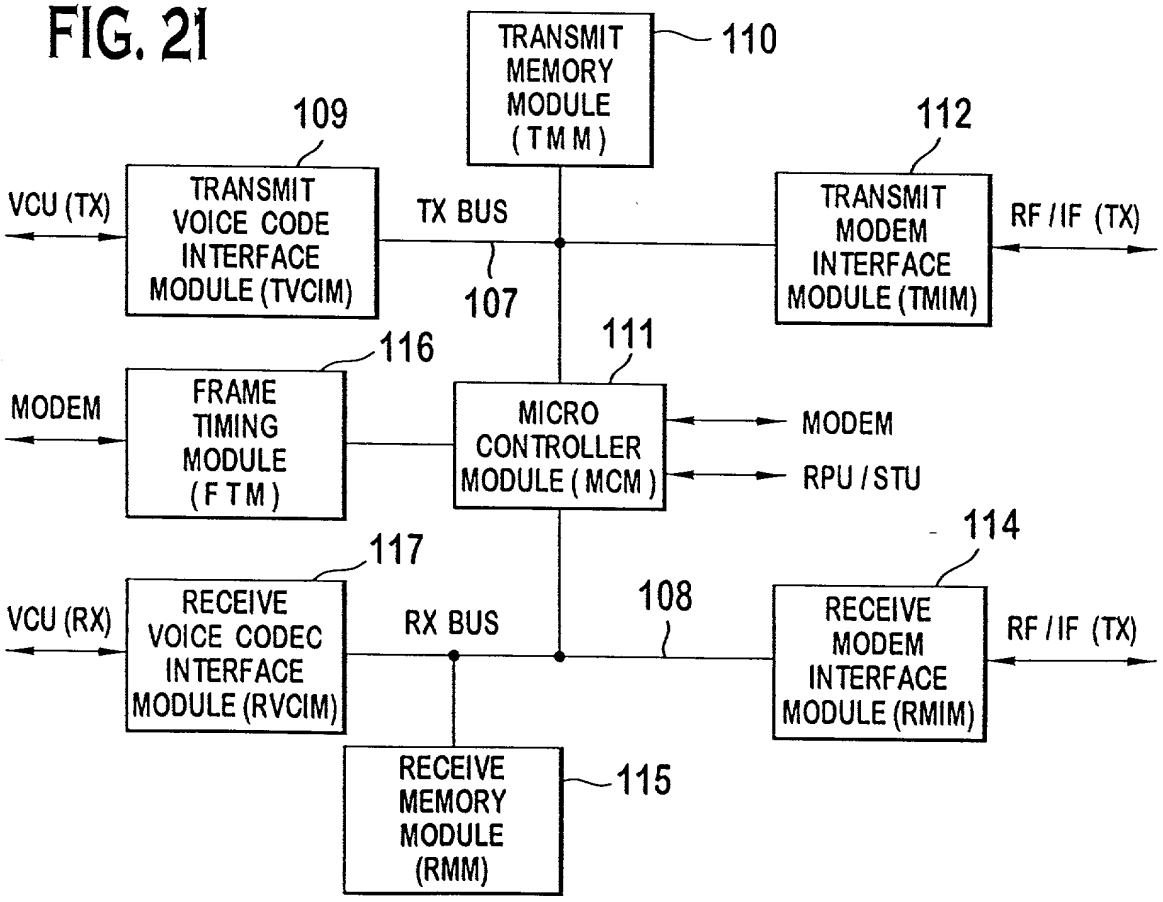

TRANSMIT MEMORY MODULE (TMM)
110
109
112
VCU (TX)
TRANSMIT VOICE CODE INTERFACE MODULE (TVCIM)
TX BUS
107
TRANSMIT MODEM INTERFACE MODULE (TMIM)
RF / IF (TX)
116
111
MODEM
FRAME TIMING MODULE (FTM)
MICRO CONTROLLER MODULE (MCM)
MODEM
RPU / STU
114
117
VCU (RX)
RECEIVE VOICE CODEC INTERFACE MODULE (RVCIM)
RX BUS
108
RECEIVE MODEM INTERFACE MODULE (RMIM)
RF / IF (TX)
RECEIVE MEMORY MODULE (RMM)
115

FIG. 15

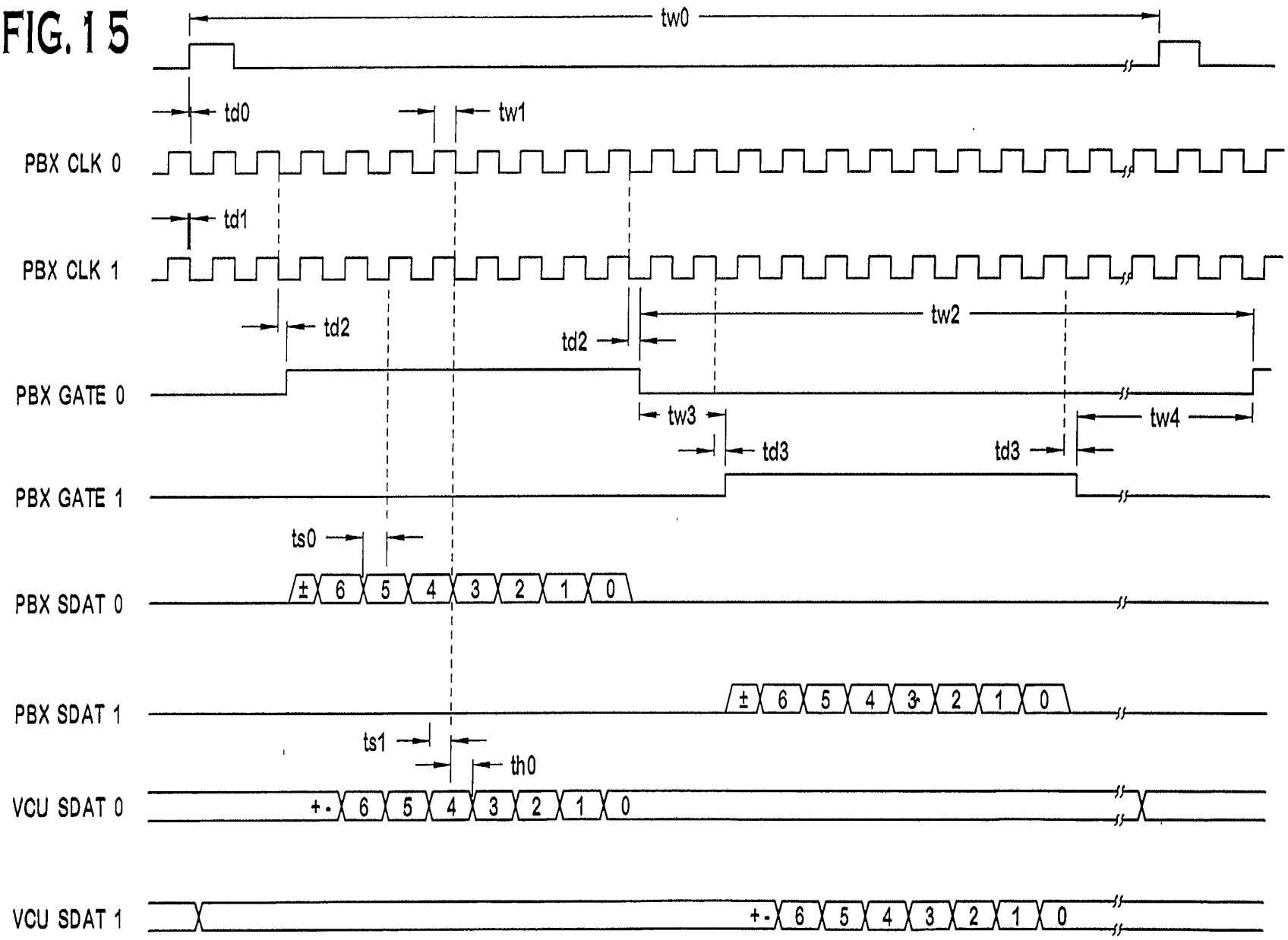

tw0
td0
tw1
PBX CLK 0
td1
PBX CLK 1
td2
td2
tw2
PBX GATE 0
tw3
tw4
td3
td3
PBX GATE 1
ts0
PBX SDAT 0
± 6 5 4 3 2 1 0
PBX SDAT 1
± 6 5 4 3 2 1 0
ts1
th0
VCU SDAT 0
+ - 6 5 4 3 2 1 0
VCU SDAT 1
+ - 6 5 4 3 2 1 0

FIG. 17

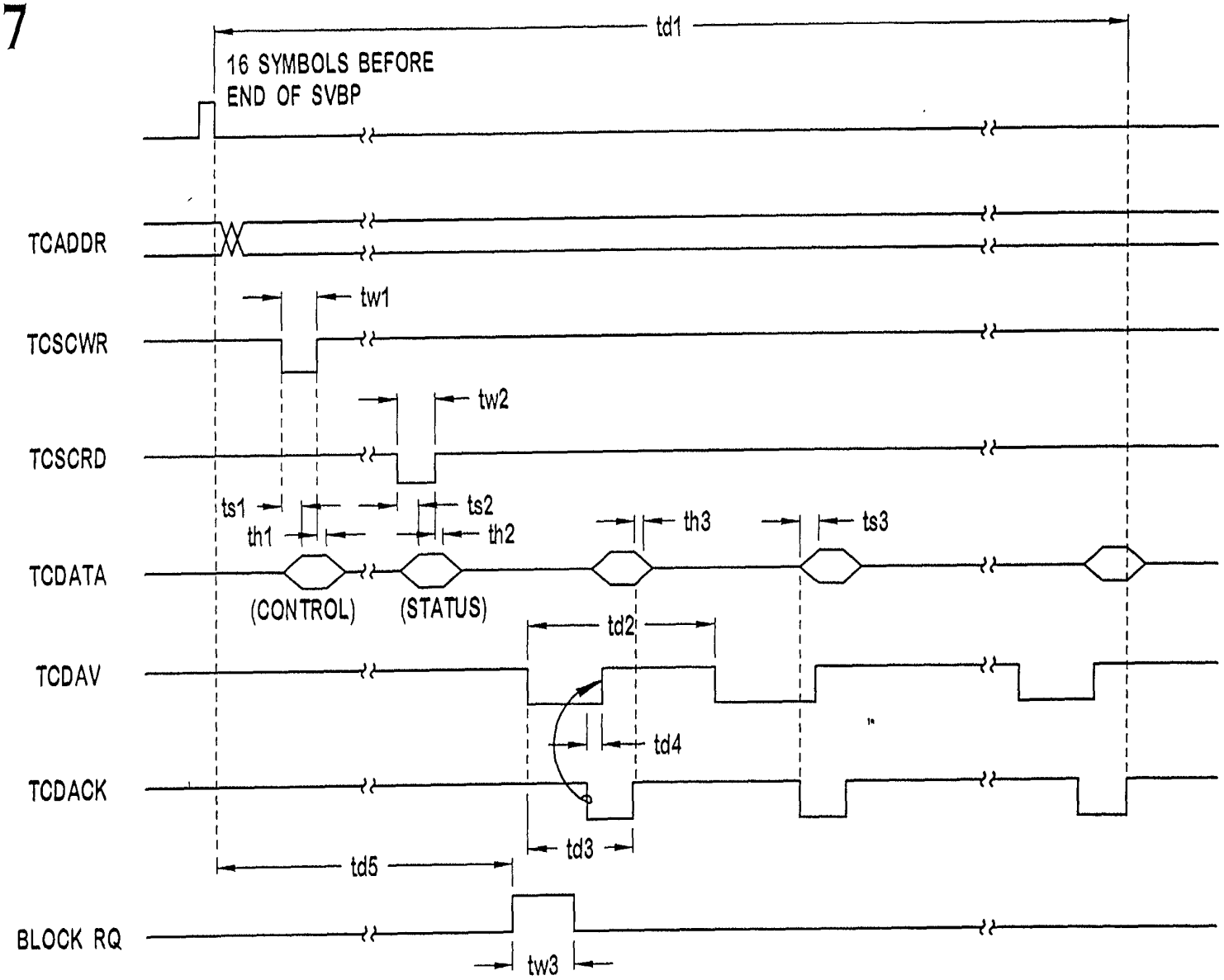
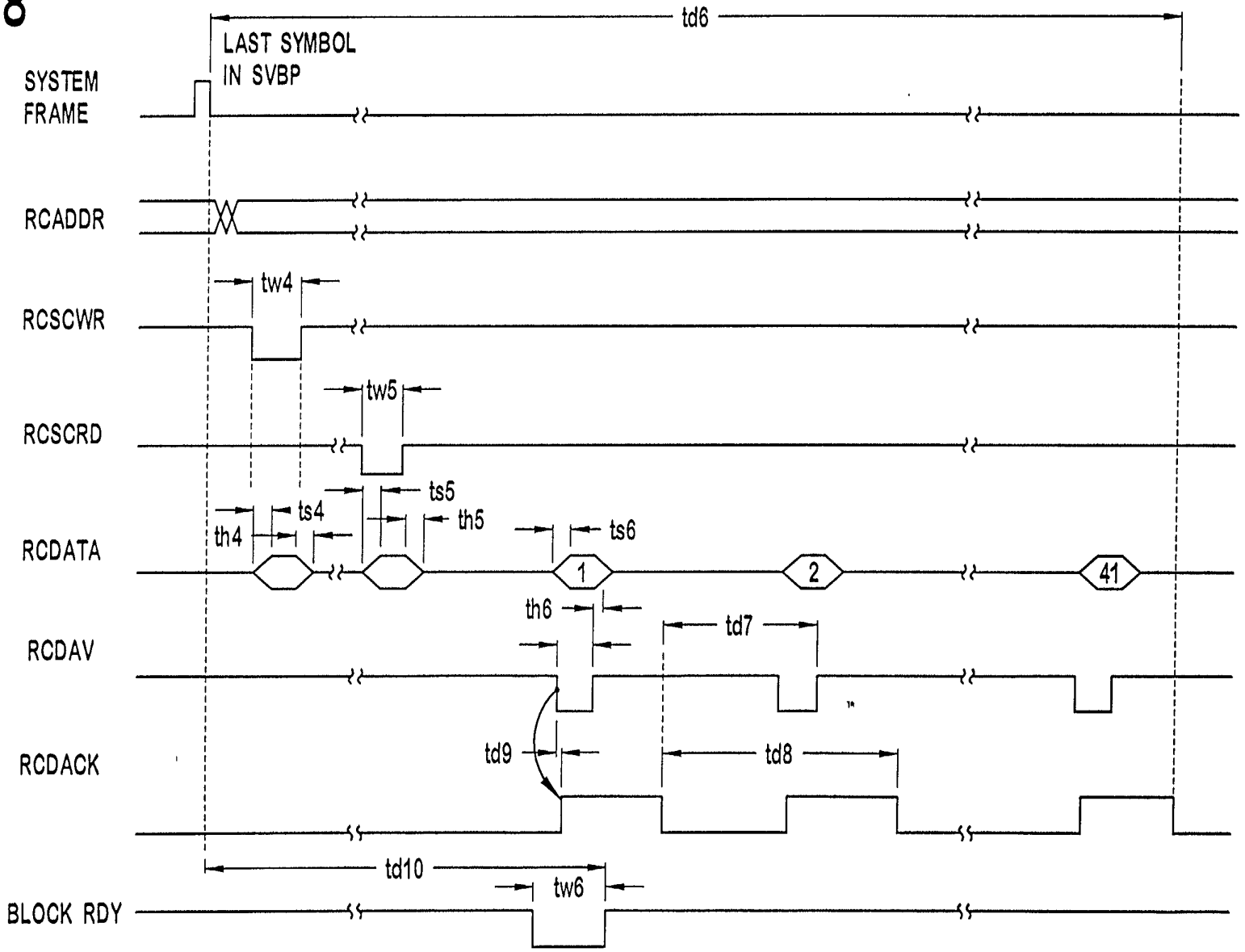

td1
16 SYMBOLS BEFORE
END OF SVBP
TCADDR
tw1
TCSCWR
tw2
TCSCRD
ts1
th1
ts2
th2
th3
ts3
TCDATA
(CONTROL)
(STATUS)
td2
TCDAV
td4
TCDACK
td3
td5
BLOCK RQ
tw3

FIG. 18


td6
LAST SYMBOL
IN SVBP
SYSTEM
FRAME
RCADDR
tw4
RCSCWR
tw5
RCSCRD
ts5
ts4
th4
th5
ts6
RCDATA
1
2
41
th6
td7
RCDAV
td9
td8
RCDACK
td10
tw6
BLOCK RDY

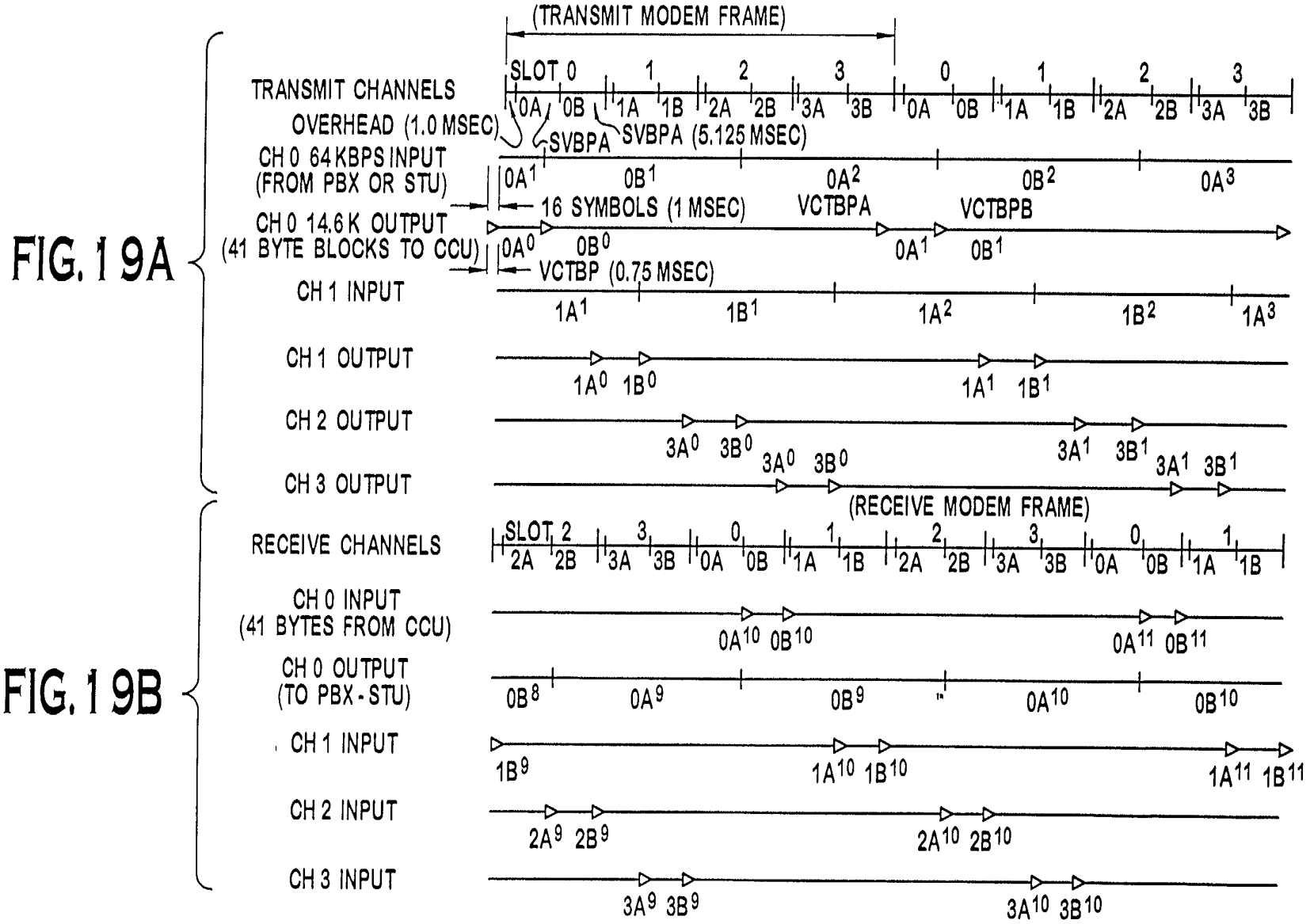


FIG. 19A

FIG. 19B

FIG. 20A

RECEIVE CHANNELS

CH 2 INPUT 14.6 KBPS
(41 BYTE BLOCK FROM CCU)

CH 2 OUTPUT 64 KBPS
(TO PBX)

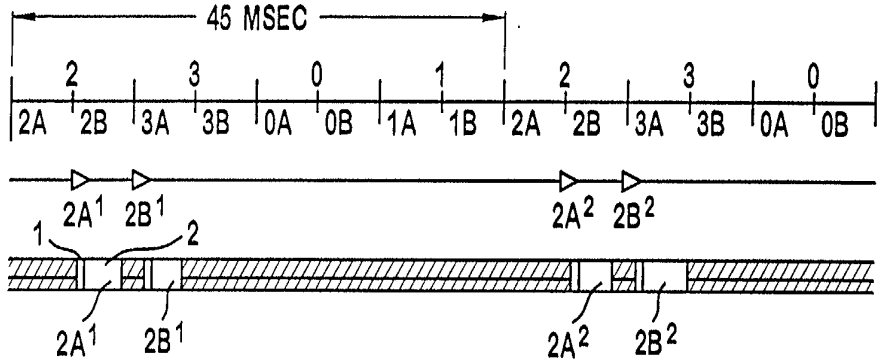


FIG. 20B

TRANSMIT CHANNELS

CH 2 INPUT 64 KBPS
(FROM PBX)

CH 2 OUTPUT 14.6 KBPS
(41 BYTE BLOCK TO CCU)

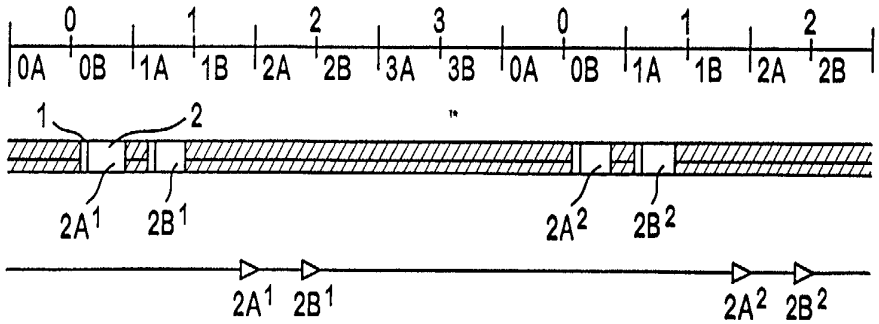


FIG. 22

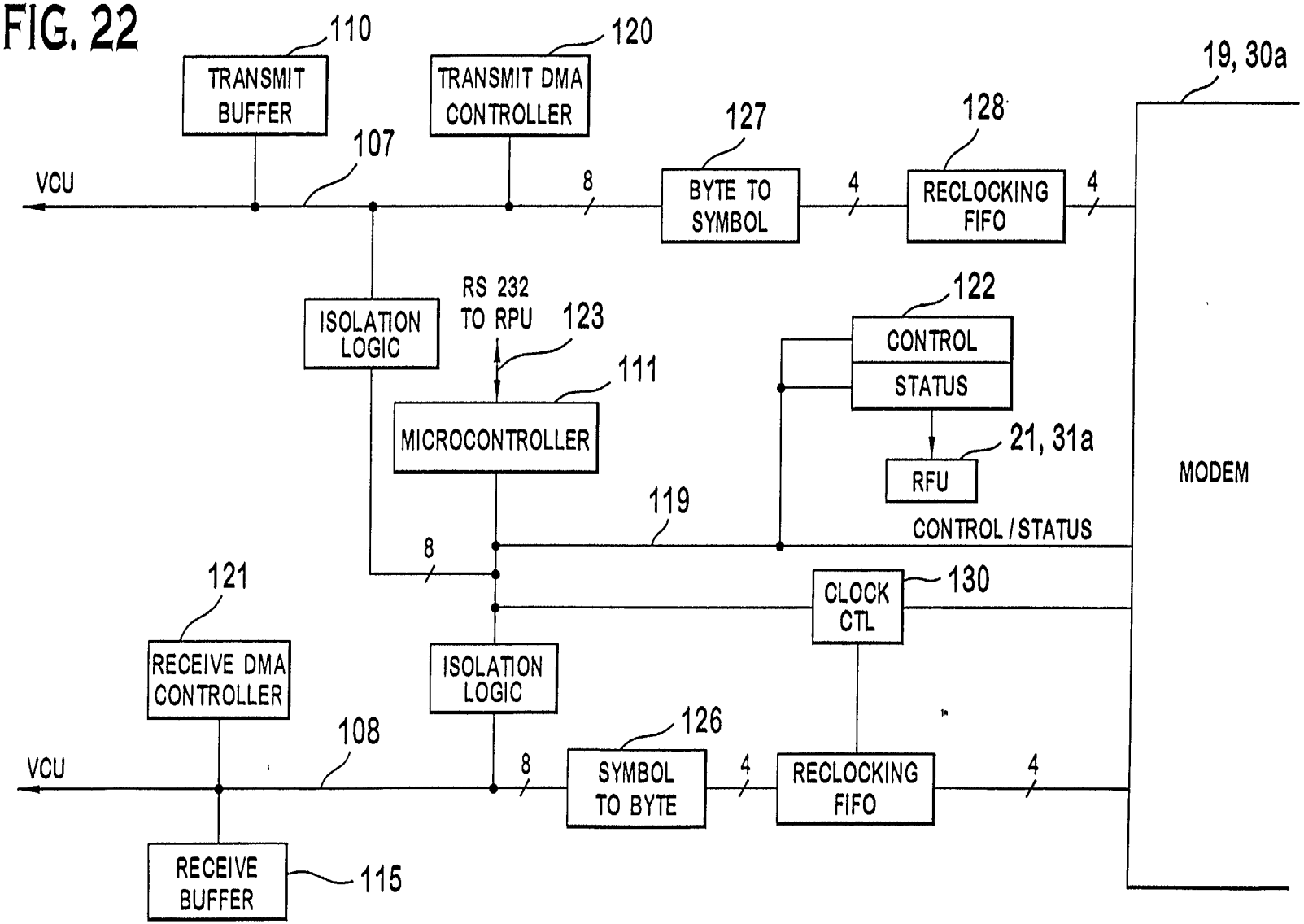

110
TRANSMIT BUFFER
120
TRANSMIT DMA CONTROLLER
19, 30a
127
128
107
VCU
8
BYTE TO SYMBOL
4
RECLOCKING FIFO
4
RS 232 TO RPU
123
122
ISOLATION LOGIC
CONTROL
STATUS
111
MICROCONTROLLER
21, 31a
RFU
MODEM
119
CONTROL / STATUS
8
121
130
CLOCK CTL
RECEIVE DMA CONTROLLER
ISOLATION LOGIC
126
108
VCU
8
SYMBOL TO BYTE
4
RECLOCKING FIFO
4
RECEIVE BUFFER
115

FIG. 23

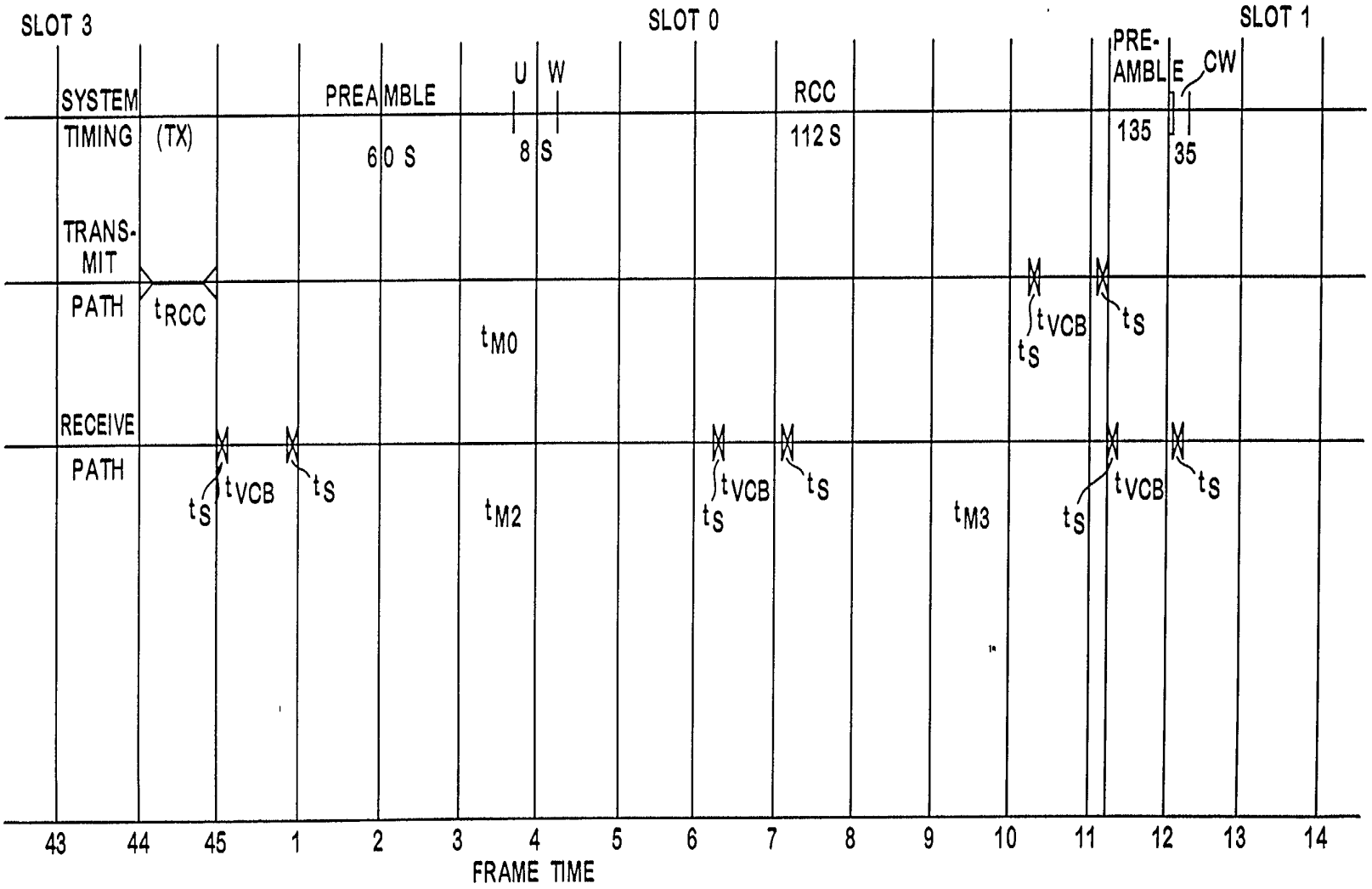
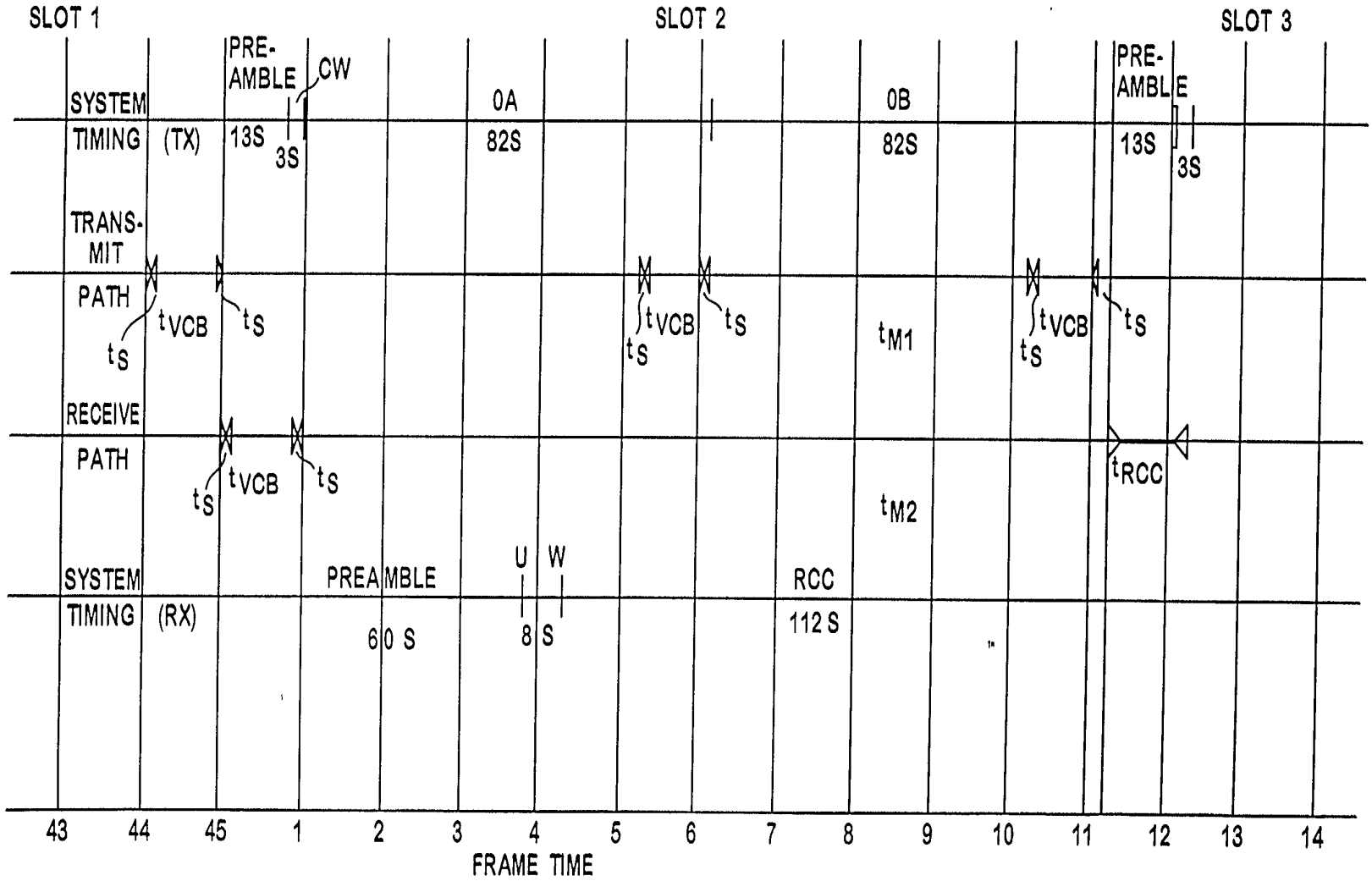

SLOT 3
SLOT 0
SLOT 1
SYSTEM TIMING
(TX)
TRANS-MIT
PATH
RECEIVE PATH
PREAMBLE
60 S
U
W
8 S
RCC
112 S
PRE-AMBLE
135
E
CW
35
tRCC
tM0
tM2
tM3
tVCB
tS
43
44
45
1
2
3
4
5
6
7
8
9
10
11
12
13
14
FRAME TIME

FIG. 24


SLOT 1
SLOT 2
SLOT 3
SYSTEM TIMING (TX)
PRE-AMBLE
CW
13S
3S
0A
82S
0B
82S
PRE-AMBLE
13S
3S
TRANS-MIT
PATH
t_S
t_{VCB}
t_S
t_S
t_{VCB}
t_S
t_{M1}
t_S
t_{VCB}
t_S
RECEIVE PATH
t_S
t_{VCB}
t_S
t_{RCC}
t_{M2}
SYSTEM TIMING (RX)
PREAMBLE
60 S
U
W
8 S
RCC
112 S
43
44
45
1
2
3
4
5
6
7
8
9
10
11
12
13
14
FRAME TIME

EP 0 530 050 A2

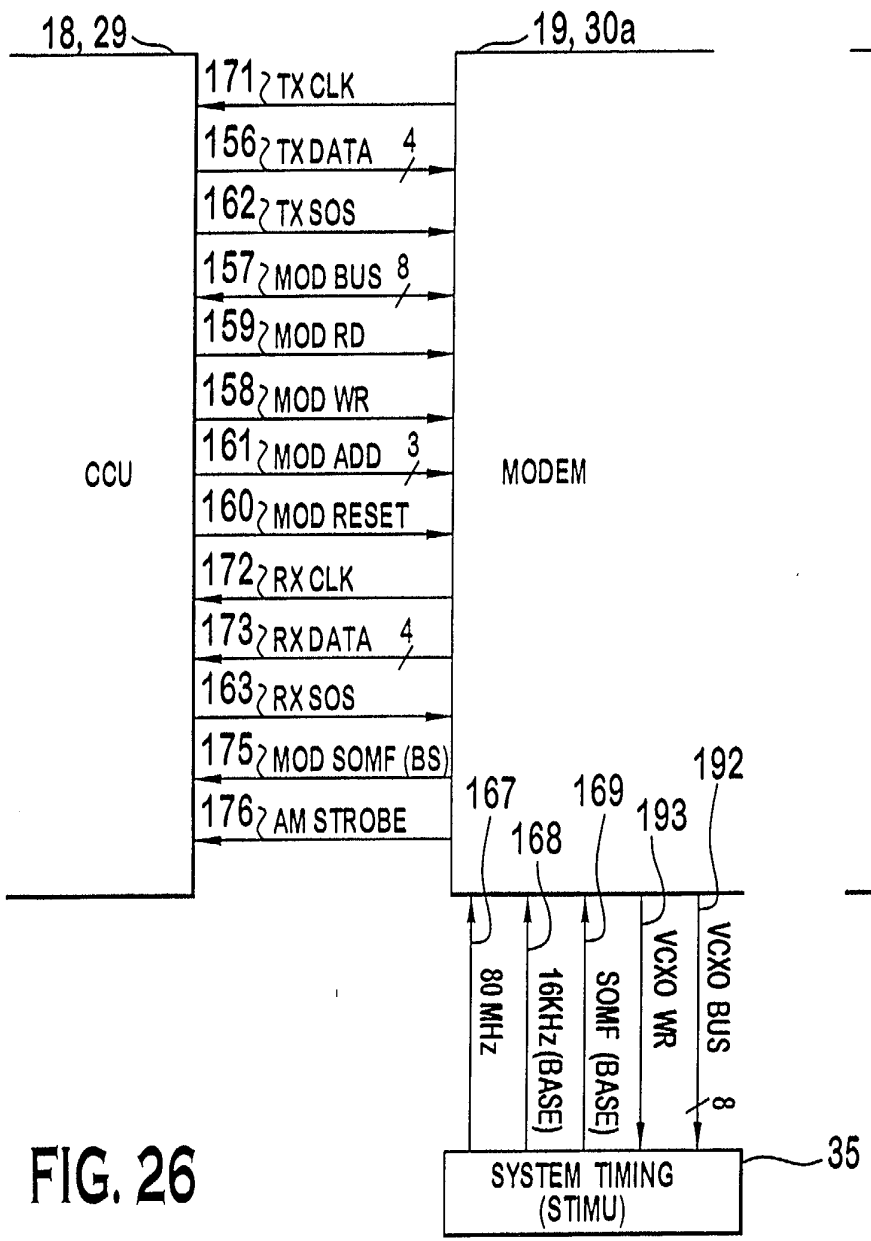


FIG. 26

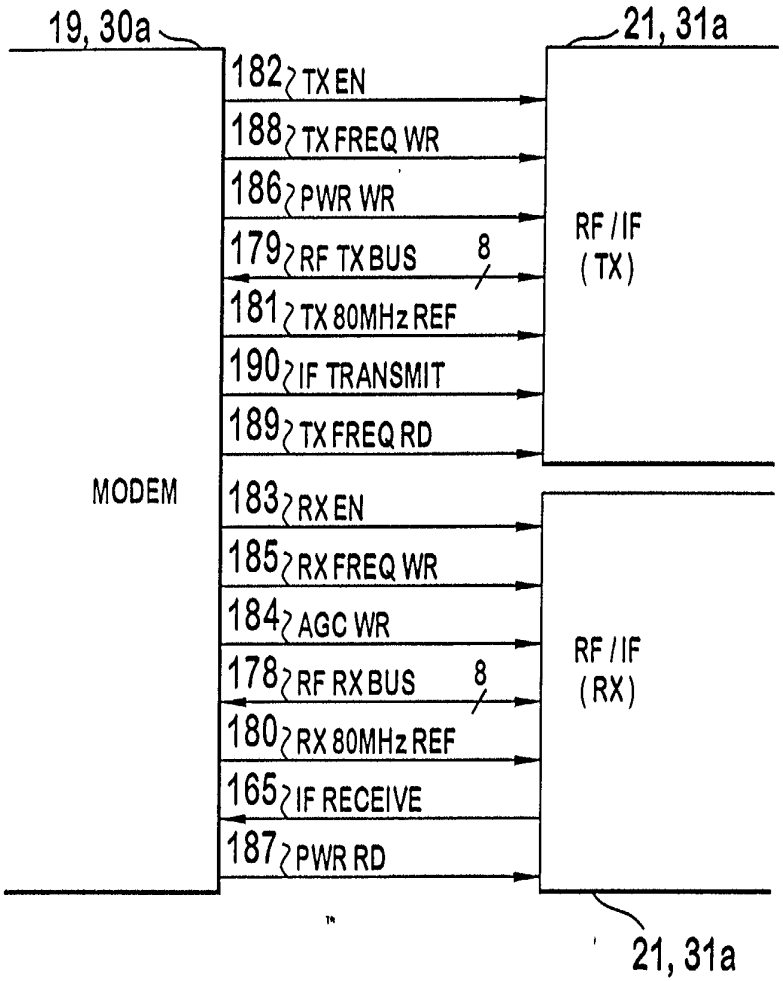


FIG. 27

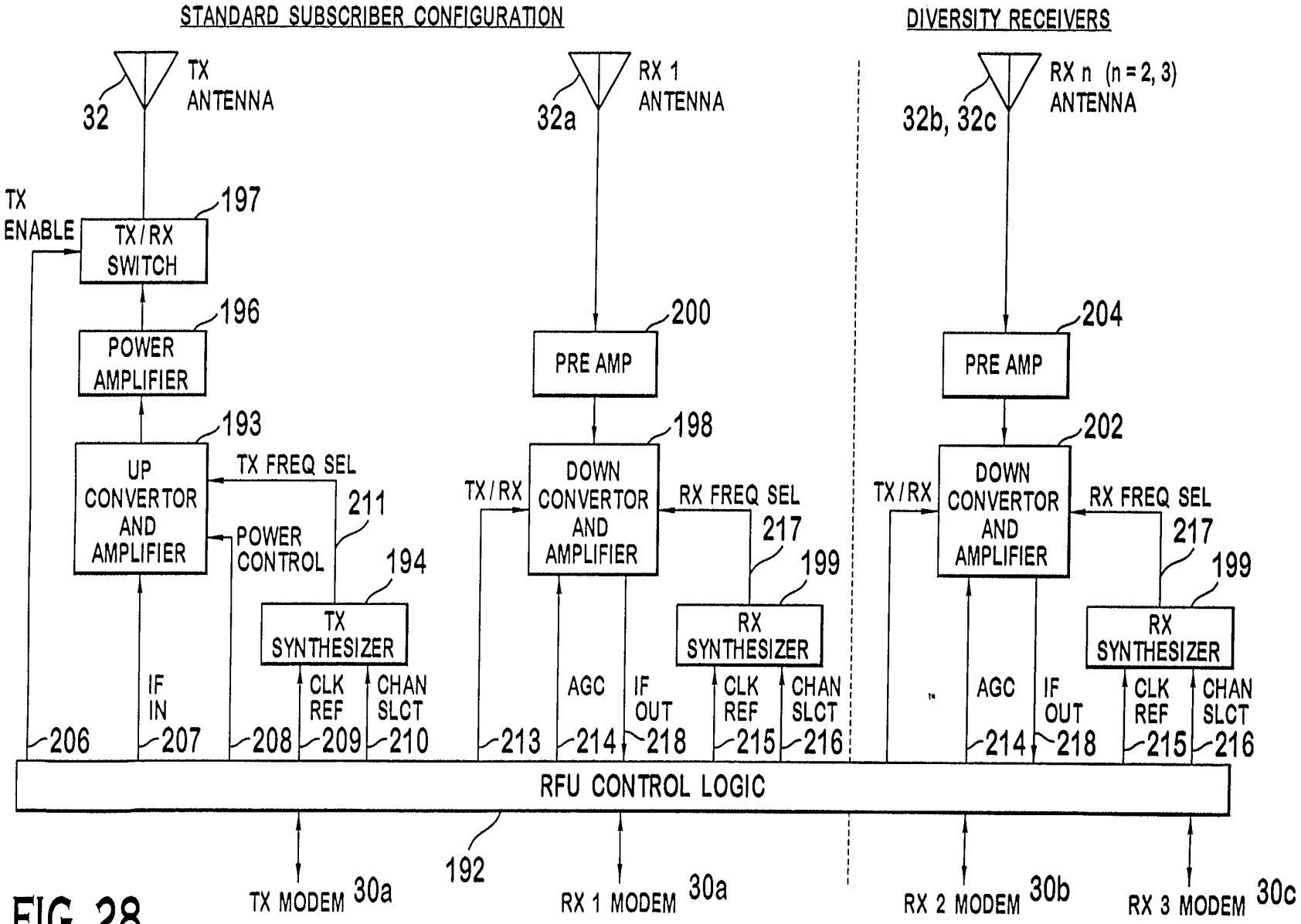

STANDARD SUBSCRIBER CONFIGURATION
DIVERSITY RECEIVERS
TX ANTENNA
32
RX 1 ANTENNA
32a
RX n (n = 2, 3) ANTENNA
32b, 32c
TX ENABLE
TX/RX SWITCH
197
POWER AMPLIFIER
196
UP CONVERTOR AND AMPLIFIER
193
TX FREQ SEL
211
POWER CONTROL
TX SYNTHESIZER
194
PRE AMP
200
DOWN CONVERTOR AND AMPLIFIER
198
TX/RX
RX FREQ SEL
217
RX SYNTHESIZER
199
PRE AMP
204
DOWN CONVERTOR AND AMPLIFIER
202
RX SYNTHESIZER
IF IN
AGC
IF OUT
CLK REF
CHAN SLCT
206
207
208
209
210
213
214
218
215
216
RFU CONTROL LOGIC
192
TX MODEM 30a
RX 1 MODEM 30a
RX 2 MODEM 30b
RX 3 MODEM 30c

FIG. 28

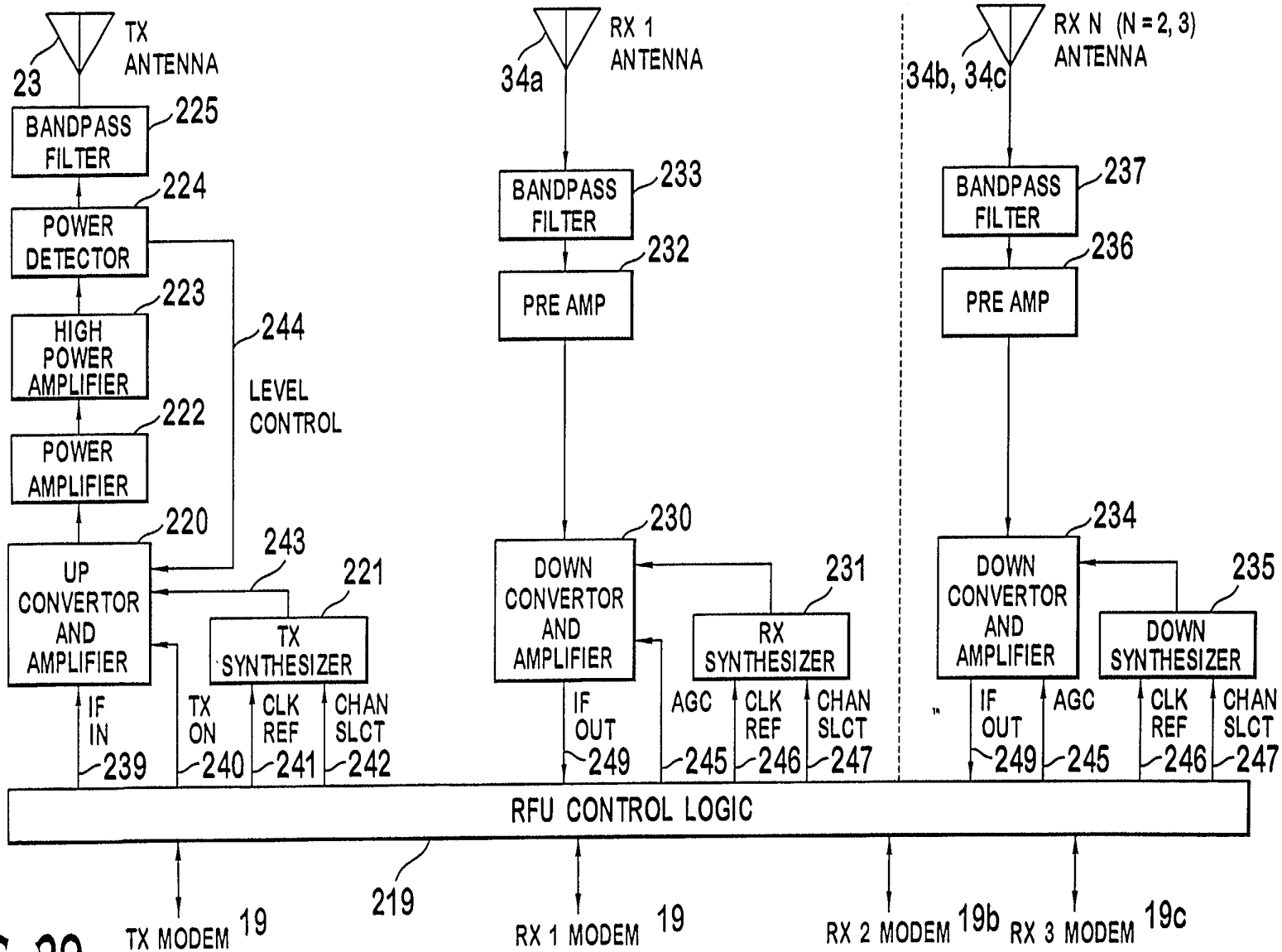

TX ANTENNA
23
BANDPASS FILTER
225
POWER DETECTOR
224
HIGH POWER AMPLIFIER
223
POWER AMPLIFIER
222
UP CONVERTOR AND AMPLIFIER
220
244
LEVEL CONTROL
243
221
TX SYNTHESIZER
IF IN
239
TX ON
240
CLK REF
241
CHAN SLCT
242
RX 1 ANTENNA
34a
BANDPASS FILTER
233
PRE AMP
232
DOWN CONVERTOR AND AMPLIFIER
230
RX SYNTHESIZER
231
IF OUT
249
AGC
245
CLK REF
246
CHAN SLCT
247
RX N (N = 2, 3) ANTENNA
34b, 34c
BANDPASS FILTER
237
PRE AMP
236
DOWN CONVERTOR AND AMPLIFIER
234
DOWN SYNTHESIZER
235
IF OUT
249
AGC
245
CLK REF
246
CHAN SLCT
247
RFU CONTROL LOGIC
219
TX MODEM 19
RX 1 MODEM 19
RX 2 MODEM 19b
RX 3 MODEM 19c

FIG. 29